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a throughput maximizing unit for processing said memory requests to the synchronous DRAM in response to scheduling which maximizes the use of data slots by the synchronous DRAM.

Cancel claim 2.

Rewrite claim 4 in independent form as follows:

3. (Amended) A controller [according to claim 1, further comprising] for a synchronous DRAM comprising:

a sorting unit for receiving memory requests and sorting said memory requests based on their addresses;

a throughput maximizing unit for processing said memory requests to the synchronous DRAM in response to scheduling which maximizes the use of data slots by the synchronous DRAM; and

a control block for receiving a controller clock signal and developing an SDRAM clock signal by dividing said controller clock signal with a programmable divisor value.

Claim 9, line 1, delete "2" and insert --1--.

10. (Twice Amended) A system for interfacing a processing device with a synchronous DRAM comprising:

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means for developing memory requests from the processing device;

means for tagging said memory requests to indicate the order in which they are provided by the processing device; and

a controller for maximizing throughput of said memory requests from the processing device to the synchronous DRAM based on scheduling constraints of the synchronous DRAM and arbitrating between conflicting memory requests so that data slots used by the synchronous DRAM are maximized.

11. (Amended) A method for controlling a synchronous DRAM comprising the steps of:

(a) receiving memory requests and sorting said memory requests based on their addresses;

(b) tagging said memory requests to indicate a sending order thereof before said memory requests are received at said step (a); and

[(b)] (c) maximizing throughput of said memory requests to the synchronous DRAM so that use of data slots by the synchronous DRAM is maximized.

Cancel claim 14.

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Rewrite claim 16 in independent form as follows:

13. ~~16.~~ (Amended) A method [according to claim ~~13~~ 11, further comprising the steps of] for controlling a synchronous DRAM comprising the steps of:

(a) receiving memory requests and sorting said memory requests based on their addresses;

(b) maximizing throughput of said memory requests to the synchronous DRAM so that use of data slots by the synchronous DRAM is maximized; and

(c) receiving a controller clock signal and developing an SDRAM clock signal by dividing said controller clock signal with a programmable divisor value.

Claim 21, line 1, delete "14" and insert --13--.

20. ~~23.~~ (Twice Amended) A method for interfacing a processing device with a synchronous DRAM, comprising the steps of:

(a) developing memory requests from the processing device;

(b) tagging said memory requests to indicate the order in which they are provided by the processing device; and

[(b)] (c) maximizing throughput of said memory requests from the processing device to the synchronous DRAM based on scheduling constraints of the synchronous DRAM and arbitrating between conflicting memory requests so that the data slots used by the synchronous DRAM are maximized.

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